**REMARKS**

Claims 1-37 were pending in the application. Claims 1, 10, 13, 19, 21-23 and 31-33 have been amended. Claims 38-43 have been added. Claims 1-43 are currently pending in the application.

**35 U.S.C. § 112 Rejections:**

Claims 23 and 33 were rejected under 35 U.S.C. § 112, first paragraph as failing to comply with then enablement requirement. The Examiner asserts that the claims contain subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which t is most nearly connected, to make and/or use the invention, without undue experimentation. Regarding claims 23 and 33, the Examiner asserts that it is unclear as to what the functionality is of "setting the first timer flag when the first timer flag has not been set and setting a second timer flag when the second timer when the second timer flag has not been set." Applicant respectfully traverses this rejection.

Applicant submits that the functionality recited in claims 23 and 33 is clearly and concisely explained in paragraph [0047] of the published version of the present application (U.S. Patent Application Publication No. 2003/0084364), which states:

> "[0047] However, if the free-running timer 450 detects (at 520) at least one entry in the locations 410(1-m) then the free-running timer 450 may examine (at 550) the first timer flag 413(1-m). If the first timer flag 412(1-m) has not been set, that may indicate that the transaction stored in the location 410(1-m) may have been initiated in the previous cycle of the free-running timer 450. In that case, the free-running timer 450 may set (at 560) the first timer flag 412(1-m). If the first timer flag 412(1-m) has been set, indicating that the transaction may have been idle for more than one cycle of the free-running timer 450, the free-running timer 450 **may** set (at 570) the second timer flag 413(1-m) to indicate that the corresponding data transaction may have been idle for **substantially** more than one timer cycle.

It may then be desirable to initiate a data timeout sequence for that transaction." (Emphasis added).

The functionality provided by setting these flags is further explained in paragraph [0048], which states:

> "[0048] Referring back now to FIG. 4, the first and second timer flags 412(1-m), 413(1-m) may, in one embodiment, be coupled to one of a plurality of logic gates 460(1-m), which may be coupled to a multiplexer 470. When the free-running timer 450 has set **both the first and the second timer flags** 412(1-m), 413(1-m) of one of the plurality of locations 410(1-m), the corresponding logic gate 460(1-m) may assert a positive signal to the multiplexer 470. The multiplexer 470 may, in one embodiment, use the positive assertion to initiate a data time-out sequence." (Emphasis added)

Accordingly, Applicant submits that the functionality provided by "setting the first timer flag when the first timer flag has not been set and setting the second timer flag when the first timer flag has been set" is described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention, without undue experimentation. Accordingly, Applicant respectfully requests removal of the 35 U.S.C. § 112 first paragraph rejection.

Claims 21 and 31 were rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to point out and distinctly claim the subject matter which Applicant regards as the invention. Claims 21 and 31 have been amended. Applicant submits that the amended versions of these claims are in compliance with 35 U.S.C. § 112, second paragraph, and thus respectfully requests removal of the rejection.

**35 U.S.C. § 103 Rejections:**

Claims 1-4, 6-9, 11-21, 26-31 and 35-37 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Talluri, U.S. Patent 6,014,710 and Bunton, U.S. Patent 6,374,282. Claims 10, 22-25, and 32-34 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Talluri and Bunton and in further view of Doing, U.S. Patent 6,018,759. Claim 5 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Talluri in view of Wilson, U.S. Patent 6,718,413. Applicant respectfully traverses these rejections.

**The cited references, taken singly or in combination, do not teach or suggest all of the elements of the independent claims.** Talluri teaches a system and method for message transmission between network nodes using remote wires. A first computer sends a sequence of messages to a second computer using remote write operations to directly store each message in a corresponding memory location in the second computer, without performing remote read operations to confirm storage of each message in the second computer's memory. The first computer detects message transmission errors, if any, during the transmission of each message to the second computer and when a message transmission error is detected, resends the message to the second computer. The first computer also sends trigger messages to the second computer to prompt the second computer to process messages stored in the second computer's memory. The second computer processes each received message and uses a remote write operation to store an acknowledgment message in a corresponding memory location in the first computer. The first computer, upon detecting a failure to receive the acknowledgment message corresponding to any of the previously sent messages, undertakes remedial actions to determine whether the second computer has processed each of the unacknowledged previously sent messages. When the remedial actions determine that the second computer has not processed the unacknowledged previously sent message, the first computer prompts the second computer to process the unacknowledged previously sent message.

Bunton teaches a network protocol that provides multi-threaded transaction processing by keeping track of the status of a plurality of independent outstanding requests. Time-out data for multiple independent transactions is maintained by a transaction layer protocol (TLP). A time-out of a transaction is utilized to invalidate the transaction

Doing teaches a method, apparatus, and article of manufacture for performing thread switch tuning for optimal performance of a program executed by a computer data processing system having a multithreaded processor. The system includes a performance monitor facility; a thread switch controller enabling thread switching for the target program while the target program is executed and disabling thread switching after completing execution of the target program; a thread switch control register including at least one thread switching event for the target program; a monitor for monitoring performance of the target program by the performance monitor facility to measure and record the performance, setting a different value for the thread switch control register whereby the target program is executed for the plurality of times, each time with a different value for the thread switch control register, choosing one of the values of the thread switch control register, after completing execution of the target program for the plurality of times, as an optimal value of the thread switch control register for the target program, based on a highest performance recorded by the performance monitor facility.

In contrast, Applicant's independent claim 1 recites, in pertinent part:

> "a scoreboard comprising a plurality of locations adapted to store transaction identifiers each associated with a transaction, wherein each transaction comprises a first client sending a request to a second client, and wherein each transaction identifier includes a first timer flag and a second timer flag" (Emphasis added).

Independent claims 13, 19, and 31 recite similar combinations of features.

None of the cited references, taken singly or in combination, teach or suggest this combination of features. In the office action, the Examiner asserts that Doing teaches transaction identifiers comprising a first and second timer flag in Col. 5, line 55 to Col. 6, line 42. Applicant respectfully disagrees with the Examiner's characterizations for the following reasons.

In column 6, lines 15-23, Doing states:

> "The invention is also a method of computer processing, comprising setting a first time-out value in a first time-out register, executing a first thread of instructions in a multithreaded processor, resetting a first time-out counter when a thread switch occurs away from the **first thread**, incrementing the first time-out counter every period the **first thread** is unable to execute, sending a first time-out signal to a thread switch controller when the first time-out register is equivalent to the first time-out value." (Emphasis added)

In column 6, lines 25-38, Doing states:

> "In addition, the processor may have a second time-out register **for a second thread** which may have a different time-out value than the first time-out value. In any event, the time-out values can be gaged to be longer than the most frequent longest latency period in which the threads are inactive, such as accessing main memory. So, the invention also comprises a method of setting a second time-out value, resetting a second time-out counter when a thread switch occurs away from a **second thread**, incrementing the second time-out counter every time period the **second thread** is unable to execute, then sending a second time-out signal to the thread switch controller when the second time-out register is equivalent to the second time-out value." (Emphasis added)

From the citations of Doing presented above, it is clear that the first time-out value is associated with a first thread, while a second time-out value is associated with a second

thread. Thus, the first and second time-out values are not associated with the same thread, and thus do not teach or suggest **a** transaction identifier associated with **a** transaction, wherein the transaction identifier includes a first timer flag **and** a second timer flag. Furthermore, Applicant respectfully disagrees with the Examiner's interpretation of a thread as a transaction as recited in Applicant's independent claims, as Applicant's independent claims clearly recite a transaction comprising a first client sending a request to a second client. Applicant submits that Doings teachings are directed to threads executing in a computer processor, and are thus not equivalent to a first client sending a request to a second client. Thus, Applicant submits that the Tarulli, Bunton, and Doing, taken either singly or in combination, do not teach or suggest all of the elements of the independent claims.

For at least these reasons, Applicant submits that a case of obviousness has not been established, and thus respectfully requests removal of the 35 U.S.C. § 103(a) rejections.

**Patentability of the Added Claims:**

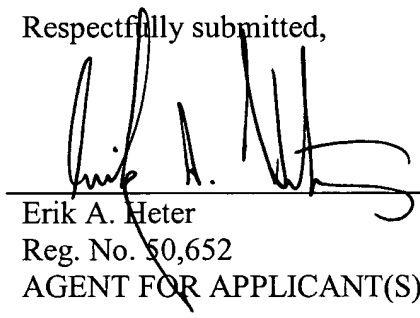
The present amendment adds claims 38-43. Claims 38-40 depend from claim 1, while claims 41-43 depend from claim 13, and are thus believed allowable for at least the same reasons. Applicant submits that no new matter has been added, and further submits that the newly added claims are fully supported in the specification, e.g., in paragraph [0047] of the published version of the present application (U.S. Patent Application Publication No. 2003/0084364).

## CONCLUSION

Applicant submits the application is in condition for allowance, and an early notice to that effect is requested.

If any fees are due, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C. Deposit Account No. 501505/5681-49700/EAH.

Respectfully submitted,



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